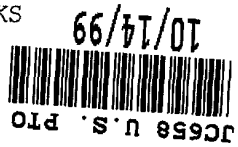
THE COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

Docket No. TSMC98-684/685/688



Sir:

Transmitted herewith for filing is the Patent Application of:

Inventor: **SYUN-MING JANG, CHUNG-SHI LIU AND CHEN-HUA YU**

For: **DAMASCENE METHOD EMPLOYING COMPOSITE ETCH STOP LAYER**

Enclosed are:

[X] 3 sheets of drawing(s) - formal.

[X] An assignment of the invention to **Taiwan Semiconductor Manufacturing Company**

[ ] An associate power of attorney

The filing fee has been calculated as shown below:

	(Col. 1)	(Col. 2)	OTHER THAN A SMALL ENTITY	
FOR:	NO. FILED	NO. EXTRA	RATE	FEE
BASIC FEE				$ 760.
TOTAL CLAIMS	20 -20=	0	x 18 =	$ 0.
INDEP CLAIMS	2 -3=	0	x 78 =	$ 0.
MULTIPLE DEPENDENT CLAIM PRESENTED			+ 260 =	
			SUB TOTAL	$ 760.
			ASSIGNMENT	$40.
			TOTAL	$ 800.

[X] Please charge my Deposit Account No. 19-0033 in the amount of **$ 800.** A duplicate copy of this sheet is enclosed.

[X] The Commissioner is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. 19-0033. A duplicate copy of this sheet is enclosed.

[X] Any additional filing fees required under 37 CFR §1.16.

[X] Any patent application processing fees under 37 CFR §1.17.

Respectfully submitted,

GEORGE O. SAILE, REG. NO. 19,572

TSMC 98-684/85/88

DAMASCENE METHOD EMPLOYING COMPOSITE ETCH STOP LAYER

by

S. M. Jang, C. S. Liu, and C. H. Yu

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to the field of conductor layers for interconnection within microelectronics fabrications. More specifically, the invention relates to the field of damascene methods for forming interconnection layers within microelectronics fabrications.

2. Description of the Related Art

Microelectronics fabrications employ conductor layers formed into patterned lines to interconnect the devices from which the fabrications are made. As the dimensions of microelectronics fabrications have become smaller, the density of interconnections has increased and the requirements placed upon interconnections have become more stringent. The number and complexity of interconnections dictate that multiple levels of interconnections be employed in practical microelectronics fabrications. There has developed a need for multi-level interconnection wiring for microelectronics fabrications with increasing demands and constraints placed on materials and methods.

In order to avoid increased electrical resistance as dimensions and hence conductor cross-sectional areas decrease, the art of microelectronics fabrication has resorted to conductor materials having higher electrical conductivity, such as, for example, copper. In addition, methods to reduce electrical resistance at contact areas between interconnection levels and via contacts have been pursued. Finally, fabrication methods and materials for forming multi-level interconnection layers which afford surface planarity as the number of interconnection levels increases have been developed, since the patterning of conductor layers by subtractive etching of conductor layers formed over surfaces leads to resulting raised surface profiles of the patterned conductor layer, which may cause subsequent fabrication problems and lead to reliability concerns.

Methods and materials providing high density interconnections with low electrical resistance have been developed which are generally satisfactory for meeting the requirements of microelectronics fabrications. These include forming the interconnection layer patterns from copper metal because of its intrinsically high electrical conductivity. The copper lines may be formed within depressions or trenches within a dielectric layer employing the method of "damascene" or inlaid pattern formation to provide a co-planar surface of the inlaid copper line pattern and the surrounding dielectric layer. Such trench patterns are often etched into an inter-level metal dielectric (IMD) layer employing photolithographic methods including an etch stop layer formed over the underlying via contact hole filled with a conductor material "stud" or "plug" to form a damascene stacked conductor interconnection layer. Such damascene stacked conductor interconnection layers are not without problems, however.

For example, the use of copper metal as the via contact hole fill or stud to form an integral damascene stacked conductor layer is not feasible at the first level of contact, to the semiconductor device itself, since copper acts as a deleterious material in semiconductor devices with degrading effect on device operation. Thus it is necessary to employ a different metal such as tungsten for the via contact hole stud. In forming contact between the overlying copper layer and the tungsten stud, there are difficulties with conventional chemical mechanical polish (CMP) planarization of the tungsten stud and subsequent formation and etching of an IMD layer in which

the copper lines are to be inlaid. This is particularly true if the planarization of the tungsten stud by harsh chemical exposure removes or damages the etch stop layer needed for the trench etching.

It is therefore towards the goal of forming improved multi-level conductor layers employing damascene methods and various conductor materials that the present invention is more generally directed.

Various methods have been disclosed for formation of damascene interconnection conductor layers with etch stop layers within semiconductor microelectronics fabrications.

For example, Kano, in U.S. Patent No. 5,380,679, discloses a method for forming a multi-level conductor wiring structure in a microelectronics fabrication affording improved adhesion between layers with no additional photolithographic steps. The method employs an intermediate bonding conductor layer to improve adhesion between the component sub-layers which form the main part of the multilevel conductor structure. The conductor layers are formed by electroplating.

Further, Woo et al., in U.S. Patent No. 5,451,543, disclose a method for forming vertical sidewalls when etching via contact holes through intermediate dielectric layers over conductor lines and lands. The method employs an etch stop layer which prevents resputtering which tends to form non-vertical sidewall profiles.

Finally, Cronin, in U.S. Patent 5,818,110, discloses a method for forming multi-layer dual damascene interconnection layers without requiring interlock vias. The method employs etched via contact hole at locations such that wide and narrow openings are available. When refilled with a conformal deposited conductor layer of appropriate thickness, the narrow openings are completely gap filled, while the wide openings are only partially filled with central openings. Subsequent CMP planarization leaves the narrow holes filled with a conductor plug to the next conductor level, while the wide holes are non-conductor filled and not available for next-level interconnection.

Desirable in the art of microelectronics fabrication are additional methods for fabrication of improved multi-level conductor interconnection structures wherein there is formed a low resistance, high strength bond between the via hole contact conductor plug and the inlaid conductor wiring layer. Also desirable are damascene methods of formation whereby the underlying conductor plug and etch stop layer experiences limited damage during formation of the damascene structure.

It is towards these goals that the present invention is generally directed.

SUMMARY OF THE INVENTION

A first object of the present invention is to provide a method for forming a damascene multi-level conductor interconnection layer upon a substrate employed within a microelectronics fabrication with improved properties.

A second object of the present invention is to provide a method for forming a damascene multi-level conductor interconnection layer in accord with the first object of the present invention, where the conductor interconnection layer is formed of multi-level conductor materials for the underlying conductor stud portion and the overlying inlaid portion of the damascene conductor layer with attenuated degradation of the conductor layers due to processing conditions.

A third object of the present invention is to provide in accord with the first object of the present invention, and the second object of the present invention, a method which is readily commercially implemented.

In accord with the objects of the present invention, there is provided a method for fabrication within a substrate employed within a microelectronics fabrication a damascene interconnection method with inhibited/attenuated damage to a conductor stud layer accessed within a trench when forming the interconnection trench pattern within a dielectric layer overlying the stud layer. To practice the invention, there is first provided a substrate having a contact region formed therein employing a first intermediate metal dielectric (IMD) layer having a pattern of via contact holes etched through the IMD layer filled with studs of conductor material. There is then planarized the surface of the IMD contact region. There is then formed over the planarized first IMD layer contact region a blanket composite etch stop layer. There is then formed over the blanket composite etch stop layer a second inter-level metal dielectric (IMD). A photoresist mask of the interconnection layer trench pattern is then formed and employed to transfer the trench pattern by subtractive etching into the second IMD dielectric layer to the upper sub-layer of the composite etch stop layer by a first etching environment. The interconnection trench pattern is then transferred through the lower sub-layer of the composite etch stop layer by subtractive etching with a second etching environment, employing the first IMD as an etch mask. A barrier metal layer is formed over the substrate. The trench pattern is then filled with a second conductor material to complete the damascene multi-layer conductor interconnection layer, with improved properties and attenuated degradation effects due to processing on the multi-layer damascene conductor structure.

The substrate employed within the microelectronics fabrication of the present invention may be a substrate employed within an integrated circuit microelectronics fabrication, a charge coupled device microelectronics fabrication, a solar cell microelectronics fabrication, a light-emitting diode microelectronics fabrication, a ceramics substrate microelectronics fabrication or a flat panel display microelectronics fabrication, where the substrate may be formed from a microelectronics conductor material, a microelectronics semiconductor material or a microelectronics dielectric material.

The method of the present invention employs methods and materials which are known in the art of microelectronics fabrication, but in a novel order and sequence. Therefore the method of the present invention is readily commercially implemented.

BRIEF DESCRIPTION OF THE DRAWINGS

The objects, features and advantages of the present invention are understood within the context of the Description of the Preferred Embodiments, as set forth below. The Description of the Preferred Embodiments is understood within the context of the accompanying drawings, which form a material part of this disclosure, wherein:

Fig. 1, Fig. 2, Fig. 3, Fig. 4 and Fig. 5 are directed towards a general embodiment of the present invention which constitutes a first preferred embodiment of the present invention. Fig. 1 to Fig. 5 illustrate the formation within a substrate employed within a microelectronics fabrication a damascene multi-layer conductor interconnection layer with improved properties.

Fig. 6, Fig. 7, Fig. 8, Fig. 9 and Fig. 10 are directed towards a more specific embodiment of the present invention which constitutes a second preferred embodiment of the present invention. Fig. 6 to Fig. 10 illustrate the formation within a semiconductor substrate employed within a microelectronics fabrication a damascene multi-layer conductor interconnection layer employing various conductor materials with improved electrical properties and attenuated damage during processing.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention provides a method for forming within a substrate employed within a microelectronics fabrication a damascene multi-layer conductor interconnection layer employing conductor materials with improved electrical properties and attenuated degradation from processing steps.

First Preferred Embodiment

Referring now to Fig. 1 to Fig. 5, there is shown a series of schematic cross-sectional diagrams illustrating various stages in the formation of a microelectronics fabrication in accord with a general embodiment of the present invention which constitutes a first preferred embodiment of the present invention. Fig. 1 is a schematic cross-sectional diagram of a microelectronics fabrication at an early stage in its fabrication in accord with a first embodiment of the present invention.

Shown in Fig. 1 is a substrate 10 upon which is formed a patterned conductor layer 12. Formed over the substrate is a first inter-level metal dielectric layer (IMD) 16 through which is formed a via contact hole filled with a conductor stud 14. The upper surface of the IMD dielectric layer 16 and the conductor via stud 14 are formed into a planarized top surface 18.

With respect to the substrate 10, the substrate 10 may be the substrate itself employed in the microelectronics fabrication, or alternatively the substrate may include any of several substrate layers employed as microelectronics substrate layers. The substrate or substrate layers may be formed of microelectronics conductor materials, microelectronics semiconductor materials or microelectronics dielectric materials. Preferably, the substrate 10 is a silicon semiconductor substrate.

With respect to the patterned conductor layer 12, the patterned conductor layer 12 may be formed of microelectronics conductor materials including but not limited to metals, alloys, conductive compounds, and semiconductors employing methods known in the art of microelectronics fabrication, including but not limited to thermal vacuum evaporation methods, electron beam evaporation methods, chemical vapor deposition (CVD) methods, physical vapor deposition (PVD) sputtering methods, electrodeposition (ED) methods, ion implantation (I/I) methods and diffusion methods. Preferably the patterned microelectronics conductor layer is formed of aluminum-copper alloy material employing physical vapor deposition (PVD) sputtering.

With respect to the conductor stud material 14, the conductor stud material 14 is preferably formed employing tungsten metal. The tungsten metal of the conductor stud 14 is preferably formed employing the method of chemical vapor deposition (CVD) from tungsten hexafluoride (WF_6); alternatively the tungsten metal may be formed employing physical vapor deposition (PVD) sputtering of tungsten metal.

With respect to the dielectric layer 16, the dielectric layer 16 is a silicon containing dielectric layer formed employing materials and methods known in the art of microelectronics fabrication . Preferably the silicon containing dielectric layer 16 is formed of silicon oxide employing chemical vapor deposition (CVD) in accord with the following process: (1) silane (SiH_4) source gas at a flow rate of about 90 standard cubic centimeters per minute(sccm); (2) nitrogen carrier gas at a flow rate of about 1000 standard cubic centimeters per minute (sccm); (3) substrate temperature about 400 degrees centigrade; (4) pressure about 5 Torr; (5) power about 600 watts; and (6) frequency 100 mHz.

With respect to the planarized surface 18, the planarized surface 18 is formed by chemical mechanical polish (CMP) planarization as is known in the art of microelectronics fabrication.

Referring now to Fig. 2, there is shown a schematic cross-sectional diagram illustrating the results of further processing of the microelectronics fabrication whose schematic cross-sectional diagram is shown in Fig. 1 in accord with the first preferred embodiment of the method of the present invention . Shown in Fig. 2 is a microelectronics fabrication otherwise equivalent to the microelectronics fabrication shown in Fig. 1, but where there has been formed over the substrate 10 a first lower sub-layer 20 and a second upper sub-layer 22 to provide a composite etch stop layer formed upon the planarized surface 18. Formed over the composite etch stop layer is a blanket second dielectric layer 24 and a patterned photoresist layer 26 defining a trench interconnection pattern 25 centered overlying the conductor stud pattern 14..

With respect to the lower sub-layer 20 of the composite etch stop layer shown in Fig. 2, the lower sub-layer 20 is formed employing a silicon oxide dielectric material employing plasma enhanced chemical vapor deposition (PECVD) method . Preferably the lower sub-layer 20 is formed according to the following process: (1) silane-nitrous oxide (SiH_4-N_2O) source gas flow rate of about 90-200 standard cubic centimeters per minute (sccm); (2) gas pressure about 5 Torr; (3) nitrogen carrier gas flow rate of about 1000 standard cubic centimeters per minute (sccm); (3) temperature about 400 degrees centigrade; (4) power about 600 watts; and (5) frequency 100 mHz.

With respect to the upper sub-layer 22 of the composite etch stop layer shown in Fig. 2, the upper sub-layer 22 is formed of silicon containing dielectric material employing plasma enhanced chemical vapor deposition (PECVD) . Preferably, the upper sub-layer 22 is formed of silicon oxynitride material employing the process conditions: (1) silane (SiH_4) silicon source gas at a flow rate of about 90 standard cubic centimeters per minute (sccm); (2) nitrogen/oxygen source nitrous oxide-ammonia (N_2O-NH_3) gases at a flow rate of about 90-90 standard cubic centimeters per minute (sccm); (3) pressure of about 5 Torr; (4) nitrogen carrier gas at a flow rate of about 2000 standard cubic centimeters per minute (sccm); (5) temperature about 400 degrees centigrade; (6) power about 600 watts; and (7) frequency 100 mHz.

With respect to the blanket second dielectric layer 24 shown in Fig. 2, the blanket second dielectric layer 24 is an inter-level metal dielectric (IMD) layer. Preferably, the second IMD layer is formed of silicon oxide dielectric material employing chemical vapor deposition (CVD) in accord with the following process: (1) silane (SiH_4) silicon source gas at a flow rate of about 100 standard cubic centimeters per minute (sccm); (2) nitrogen carrier gas at a flow rate of about 2000 standard cubic centimeters per minute (sccm); (3) power about 600 watts; (4) frequency 100 mHz; (5) temperature about 400 degrees centigrade; and (6) pressure about 5 Torr. Alternatively, the second blanket IMD layer 22 may be a low dielectric constant dielectric layer formed from a low dielectric constant dielectric material as is known in the art of microelectronics fabrication.

With respect to the patterned photoresist etch mask pattern 26 defining the trench interconnection pattern 25, the patterned photoresist etch mask pattern 26 is formed employing photolithographic materials and methods as are well known in the art of microelectronics fabrication.

Referring now more particularly to Fig. 3, there is shown a schematic cross-sectional diagram illustrating the results of further processing of the microelectronics fabrication whose schematic cross-sectional diagram is shown in Fig. 2 in accord with the first preferred embodiment of the present invention. Shown in Fig. 3 is a microelectronics fabrication otherwise equivalent to the microelectronics fabrication shown in Fig. 2, but where there has been etched into and through the dielectric layer 24' and the upper second sub-layer 22' of the etch stop layer to the lower first sub-layer 20 of the etch stop layer a trench 28, employing a first subtractive etch environment 30, followed by final stripping of the photoresist etch mask pattern 26.

With respect to the first subtractive etch environment 30 shown in Fig. 3, the first subtractive etch environment 30 employs a mixture of tetrafluoromethane (CF_4), trifluoromethane (CHF_3) and oxygen as the etching gases.

Referring now more particularly to Fig. 4, there is shown a schematic cross-sectional diagram illustrating the results of further processing of the microelectronics fabrication whose schematic cross-sectional diagram is shown in Fig. 3 in accord with the first preferred embodiment of the present invention. Shown in Fig. 4 is a microelectronics fabrication otherwise equivalent to the microelectronics fabrication shown in Fig. 3, but where there has been etched through the lower sub-layer 20' the pattern of the trench 28 employing a second subtractive etch environment 31.

With respect to the second subtractive etch environment 31 shown in Fig. 4, the second subtractive etch environment 31 is a sputter etching process employing argon as the sputtering gas.

Referring now more particularly to Fig. 5, there is shown a schematic cross-sectional diagram illustrating the results of further processing of the microelectronics fabrication whose schematic cross-sectional diagram is shown in Fig. 4 in accord with the first preferred embodiment of the present invention. Shown in Fig. 5 is a microelectronics fabrication otherwise equivalent to the microelectronics fabrication shown in Fig. 4, but where there is formed over the substrate a barrier metal layer 32. There is then formed within the trench a conductor material 34 to complete the dual damascene conductor layer.

With respect to the barrier metal layer 32 shown in Fig. 5, the barrier metal layer 32 is tantalum nitride (TaN) formed employing physical vapor deposition (PVD) sputtering.

With respect to the trench fill conductor material 34, the trench fill conductor material 34 may be a low resistivity conductor material selected from the group of conductor materials including but not limited to copper and aluminum. Preferably, the low resistivity conductor metal layer is formed employing the following process: (1) TaN barrier layer 300 angstroms in thickness formed employing physical vapor deposition (PVD) sputtering; (2) copper seed layer deposition 2000 angstroms in thickness formed employing physical vapor deposition

(PVD) sputtering; (3) copper layer 8000 angstroms in thickness formed by electrochemical deposition (ECD).

The first preferred embodiment of the present invention provides a method for forming within a substrate employed within a microelectronics fabrication a damascene multi-layer conductor interconnection layer employing different conductor materials with improved electrical conductive and contact properties and attenuated degradation from chemical processing steps

Second Preferred Embodiment

Referring now to Fig. 6 to Fig. 10, there is shown a series of schematic cross-sectional drawings illustrating the results of forming in accord with a more specific embodiment of the present invention which constitutes a second preferred embodiment of the present invention a damascene multi-layer conductor interconnection layer employing various conductor materials with improved properties and attenuated degradation due to processing. Fig. 6 is a schematic cross-sectional diagram illustrating a microelectronics fabrication at an early stage in its fabrication in accord with the present invention.

Shown in Fig. 6 is a semiconductor substrate 40 upon which is formed a patterned conductor layer 42. Formed over the substrate is an inter-level metal dielectric (IMD) layer 46 through which is formed a via contact hole filled with a tungsten conductor stud 44. The upper surface of the dielectric layer 46 and the tungsten conductor stud 44 are formed into a planarized surface 48.

With respect to the semiconductor substrate 40 shown in Fig. 6, the semiconductor substrate 40 is analogous to the substrate 10 shown in Fig. 1 of the first preferred

embodiment of the present invention. Preferably, the semiconductor substrate 40 is a silicon semiconductor substrate.

With respect to the patterned conductor layer 42 shown in Fig. 6, the patterned conductor layer 42 is analogous or equivalent to the patterned conductor layer 12 shown in Fig. 1 of the first preferred embodiment of the present invention.

With respect to the tungsten conductor stud layer 44, the tungsten conductor stud material 44 is formed employing chemical vapor deposition (CVD) of tungsten from tungsten hexafluoride (WF_6).

With respect to the chemical mechanical polish (CMP) planarized surface 48 shown in Fig. 6, the chemical mechanical polish (CMP) planarized surface 48 is analogous or equivalent to the chemical mechanical polish (CMP) planarized surface 18 shown in Fig. 1 of the first preferred embodiment of the present invention.

Referring now to Fig. 7, there is shown a schematic cross-sectional diagram illustrating the results of further processing of the microelectronics fabrication whose schematic cross-sectional diagram is shown in Fig. 6 in accord with the second preferred embodiment of the present invention. Shown in Fig. 7 is a microelectronics fabrication otherwise equivalent to the microelectronics fabrication shown in Fig. 6, but wherein there has been formed over the substrate a first upper sub-layer 50 and a second lower sub-layer 52 to form a composite etch stop layer. Formed over the composite etch stop layer is a blanket dielectric layer 54. Formed over the blanket dielectric layer 54 is a patterned photoresist etch mask layer 56 providing a trench interconnection pattern 58 centered over the underlying conductor stud pattern 44.

With respect to the first lower sub-layer 50 of the composite etch stop layer shown in Fig. 7, the first lower sub-layer 50 is formed employing an organic polymer low dielectric constant spin-on-polymer (SOP) dielectric material. Preferably, the organic polymer low dielectric constant spin-on-polymer (SOP) dielectric material is a fluorinated poly (arylene ether) organic

polymer commercially available as FLARE from Allied Signal Corporation, 1349 Moffett Park Drive, Sunnyvale, CA 94089 USA, or alternately as PAE-2 from Schumacher Corporation, 1969 Palomar Oaks Way, Carlsbad, CA 92009 USA. A further alternative commercial fluorinated poly(arylene ether) organic polymer low dielectric constant spin-on-polymer (SOP) dielectric material is SILK, available from Dow Chemical Co., 1712 Building, Midland, MI 48674 USA.

With respect to the second upper sub-layer 52 of the composite etch stop layer shown in Fig. 7, the second upper sub-layer 52 is formed of a silicon containing dielectric material formed employing chemical vapor deposition. Preferably the silicon containing dielectric layer is a silicon oxynitride dielectric layer analogous or equivalent to the silicon oxynitride layer 22 shown in Fig. 2 of the first preferred embodiment of the present invention.

With respect to the blanket dielectric layer 54 shown in Fig. 7, the blanket dielectric layer 54 is an inter-level metal dielectric (IMD) layer. Preferably, the blanket dielectric layer 54 is analogous or equivalent to the blanket dielectric IMD layer 24 shown in Fig. 2 of the first preferred embodiment of the present invention.

With respect to the patterned photoresist etch mask layer 56 shown in Fig. 7, the patterned photoresist etch mask layer 56 is analogous or equivalent to the patterned photoresist etch mask layer 26 shown in Fig. 2 of the first preferred embodiment of the present invention.

Referring now to Fig. 8, there is shown a schematic cross-sectional diagram illustrating the results of further processing of the microelectronics fabrication whose schematic cross-sectional diagram is shown in Fig. 7. Shown in Fig. 8 is a microelectronics fabrication otherwise equivalent to the microelectronics fabrication shown in Fig. 7, but where there has been etched in a subtractive etching environment 60 the interconnection trench pattern 58 through the photoresist etch mask layer 56, the blanket dielectric layer 54' and the second upper sub-layer 52' to the lower first sub-layer 50 of the composite etch stop layer.

With respect to the subtractive etching environment 60 shown in Fig. 8, the subtractive etch environment 60 is analogous or equivalent to the first subtractive etch environment shown in Fig. 3 of the first preferred embodiment of the present invention.

Referring now to Fig. 9, there is shown a schematic cross-sectional diagram illustrating the results of further processing of the microelectronics fabrication whose schematic cross-sectional diagram is shown in Fig. 8 in accord with the second preferred embodiment of the present invention. Shown in Fig. 9 is a microelectronics fabrication otherwise equivalent to the microelectronics fabrication shown in Fig. 8, but where there has been etched through the lower sub-layer 50' of the composite etch stop layer the interconnection trench pattern 58 while simultaneously stripping the photoresist etch mask layer 56 in the etching/stripping environment 62.

With respect to the stripping/etching environment 62 shown in Fig. 9, the stripping/etching environment 62 employs the following process conditions: (1) oxygen gas at a pressure of about 10 Torr; (2) temperature of about 200 degrees centigrade; and (3) power of about 500 watts.

Referring now to Fig. 10, there is shown a schematic cross-sectional diagram illustrating the results of final processing of the microelectronics fabrication whose schematic cross-sectional diagram is shown in Fig. 9 in accord with the second preferred embodiment of the present invention. Shown in Fig. 10 is a microelectronics otherwise equivalent to the microelectronics fabrication shown in Fig. 9, but where there has been formed over the substrate a blanket barrier metal layer 64. Formed within the interconnection trench pattern 58 is a copper conductor layer 66 to complete the damascene interconnection conductor layer..

With respect to the barrier metal layer 64 and the copper conductor metal 66, the barrier metal layer 64 and copper conductor layer 66 are analogous or equivalent to the barrier metal layer 34 and the copper conductor layer 36 shown in Fig. 5 of the first preferred embodiment of the present invention.

The second preferred embodiment of the present invention provides a method for forming within a semiconductor substrate employed within an integrated circuit microelectronics fabrication a damascene multi-layer conductor interconnection scheme with attenuated damage to the tungsten conductor stud layer due to processing of the overlying patterned inlaid copper layer within the dielectric layers, and with improved electrical conductivity and contacts.

As is understood by a person skilled in the art, the preferred embodiments of the present invention are illustrative of the present invention rather than limiting of the present invention. Revisions and modifications may be made to materials, structures and dimensions through which is provided the preferred embodiments of the present invention while still providing embodiments which are within the spirit and scope of the present invention, as defined by the appended claims.

What is claimed is:

1. A method for forming a patterned microelectronics layer comprising:

providing a substrate having a contact region formed therein;

forming over the substrate a first lower sub-layer and a second upper sub-layer to provide a composite etch stop layer;

forming over the composite etch stop layer an inter-level metal dielectric (IMD) layer;

forming over the IMD layer a photoresist mask layer pattern of an interconnection line trench pattern centered over the contact layer and transferring the pattern by etching while employing a first etching method through the IMD layer and the second upper sub-layer of the composite etch stop layer to the first lower sub-layer of the composite etch stop layer;

etching while employing a second etch method the first lower sub-layer from the trench pattern for the interconnection lines.

2. The method of Claim 1 wherein by employing the first lower sub-layer there is avoided etching of the contact region within the first etching method.

3. The method of Claim 1 wherein the first lower sub-layer has a higher etch rate in the second etching method than the contact region;

4. The method of Claim 1 wherein forming a damascene multi-layer conductor interconnection layer is accomplished by the method further comprising:

forming a barrier metal layer over the patterned substrate; and

filling the trench pattern with a conductor material to complete the damascene multi-layer conductor interconnection layer structure.

5. The method of Claim 1 wherein the microelectronics layer is selected from the group consisting of:

microelectronics conductor layers;

microelectronics semiconductor layers;

microelectronics dielectric layers.

6. The method of Claim 1 wherein the substrate is a substrate employed within a microelectronics fabrication selected from the group consisting of:

integrated circuit microelectronics fabrications;

charge coupled device microelectronics fabrications;

solar cell microelectronics fabrications;

light-emitting diode microelectronics fabrications;

ceramic substrate microelectronics fabrications; and

flat panel display microelectronics fabrications.

7. The method of Claim 1 wherein the first lower sub-layer is formed employing a silicon oxide dielectric material formed employing plasma enhanced chemical vapor deposition (PECVD).

8. The method of Claim 1 wherein the upper second sub-layer is formed employing a silicon oxynitride dielectric material deposited employing plasma enhanced chemical vapor deposition (PECVD).

9. The method of Claim 1 wherein the contact region via conductor stud layer material is formed employing tungsten metal.

10. The method of Claim 1 wherein the inter-level metal dielectric (IMD) layer is formed employing silicon oxide dielectric material employing chemical vapor deposition (CVD).

11. The method of Claim 1 wherein the second conductor material is copper metal.

12. A method for forming a patterned microelectronics layer comprising:

providing a substrate having a contact region of tungsten metal conductor studs formed therein;

forming over the substrate a first lower organic polymer sub-layer and a second upper sub-layer to provide a composite etch stop layer;

forming over the composite etch stop layer a blanket inter-level metal dielectric (IMD) layer;

forming over the blanket IMD layer a photoresist mask layer pattern of an interconnection line trench pattern centered over the contact region and transferring the pattern while employing a first etch method through the blanket IMD layer and the second upper sub-layer of the composite etch stop layer to the first lower organic polymer sub-layer of the composite etch stop layer; and

stripping the photoresist mask pattern layer and simultaneously etching the first lower organic polymer sub-layer to complete the formation of the interconnection trench pattern centered over the tungsten metal stud contact region.

13. The method of Claim 12 wherein by employing the first lower organic polymer sub-layer there is avoided the etching of the tungsten metal stud contact region within the first etch method.

14. The method of Claim 12 wherein forming a damascene multi-layer conductor interconnection layer structure is accomplished by the method further comprising:

forming a barrier metal layer over the substrate; and

filling the interconnection trench pattern with a conductor material to complete the damascene multi-level conductor interconnection layer structure.

15. The method of Claim 12 wherein the semiconductor substrate is a silicon semiconductor substrate.

16. The method of Claim 12 wherein the first lower organic polymer sub-layer is formed employing a low dielectric constant spin-on-polymer (SOP) dielectric material.

17. The method of Claim 12 wherein the second upper sub-layer is formed employing chemical vapor deposition (CVD) of silicon containing dielectric material.

18. The method of Claim 12 wherein the inter-level metal dielectric (IMD) layer is formed of silicon oxide dielectric material employing chemical vapor deposition (CVD).

19. The method of Claim 12 wherein the conductor material employed to fill the interconnection trench is copper.

20. The method of Claim 12 wherein the barrier metal layer is formed employing tantalum nitride (TaN).

ABSTRACT OF THE DISCLOSURE

A method for forming within a substrate employed within a microelectronics fabrication a damascene multi-layer conductor interconnection layer with inhibited/attenuated damage to a conductor stud layer accessed therein within a trench, when forming the trench interconnection pattern within a dielectric layer overlying the conductor stud layer. There is provided a substrate having a contact region formed therein employing a first intermediate metal dielectric (IMD) layer having a pattern of via contact holes etched through the IMD layer filled with studs of conductor material. There is then planarized the surface of the IMD contact region. There is then formed over the planarized first IMD layer contact region a blanket composite etch stop layer. There is the formed over the blanket composite etch stop layer a second blanket inter-level metal dielectric (IMD) layer. A patterned photoresist etch mask layer formed into the interconnection trench pattern is then formed over the substrate and employed to transfer the trench pattern into the second IMD layer and the upper sub-layer of the composite etch stop layer. The interconnection trench pattern is then transferred by a second subtractive etch into the lower sub-layer of the composite etch stop layer, employing the second IMD layer as an etch mask A barrier metal layer is then formed over the substrate. The trench pattern is then filled with a second conductor material to complete the damascene multi-layer conductor interconnection layer, with improved electrical conductivity and contact properties and inhibited/attenuated degradation effects due to processing on the damascene interconnection layer.

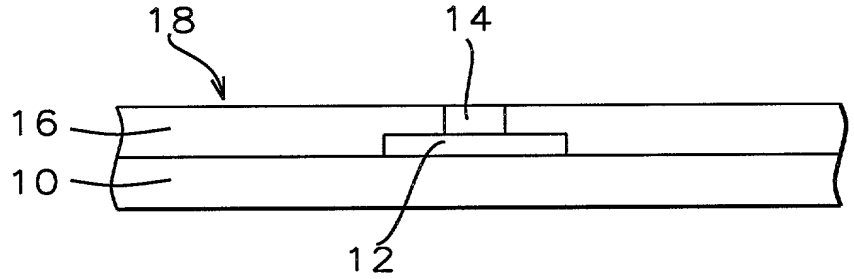


FIG. 1

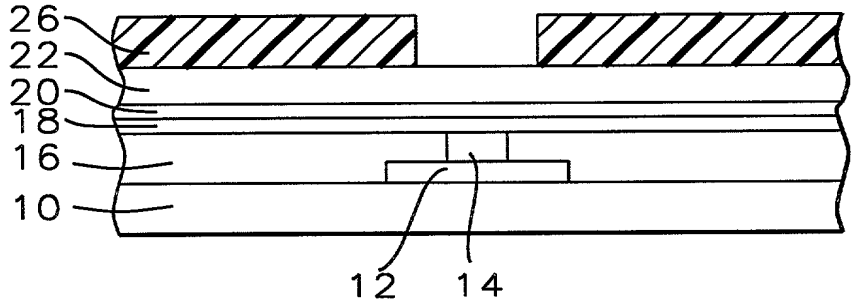


FIG. 2

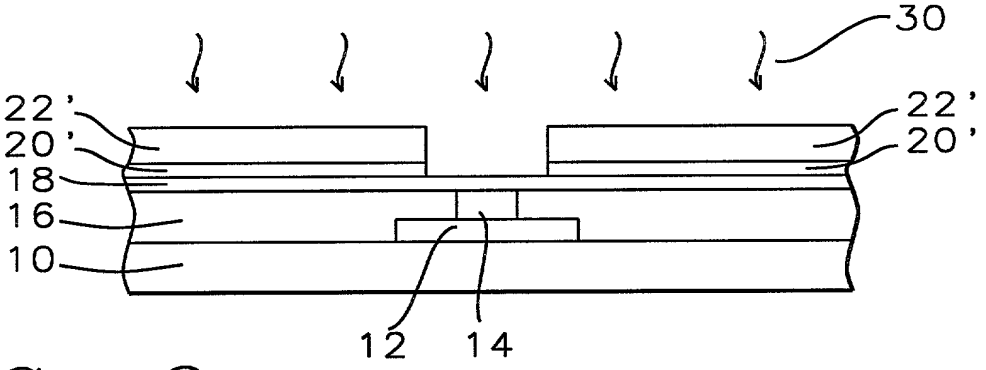


FIG. 3

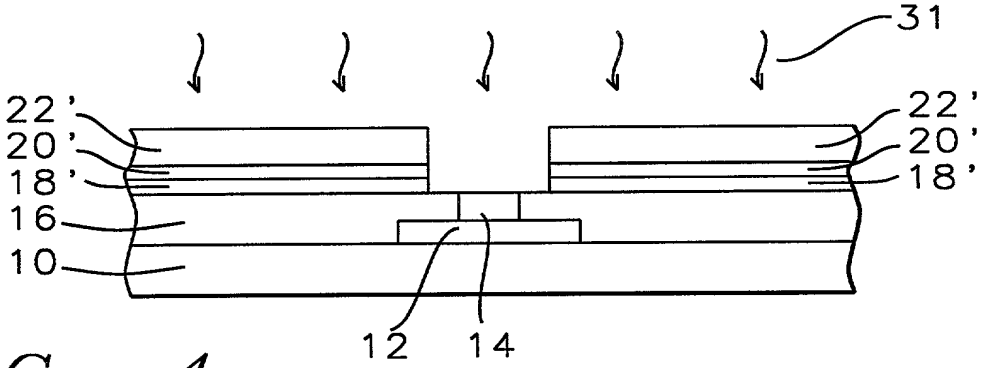


FIG. 4

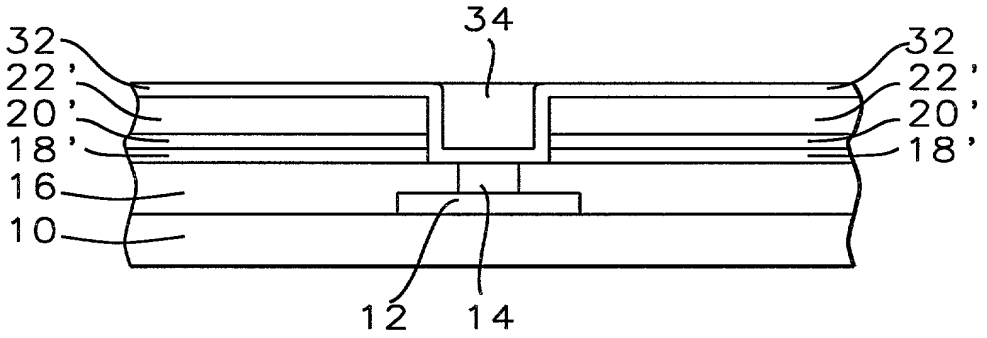


FIG. 5

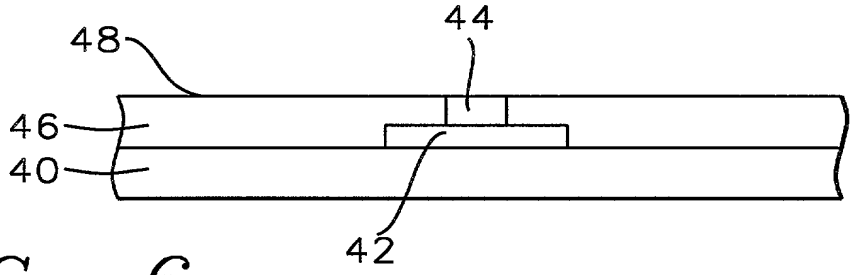


FIG. 6

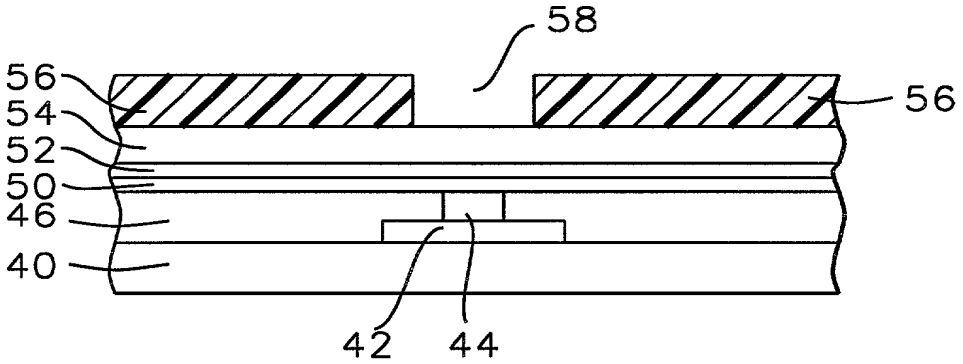


FIG. 7

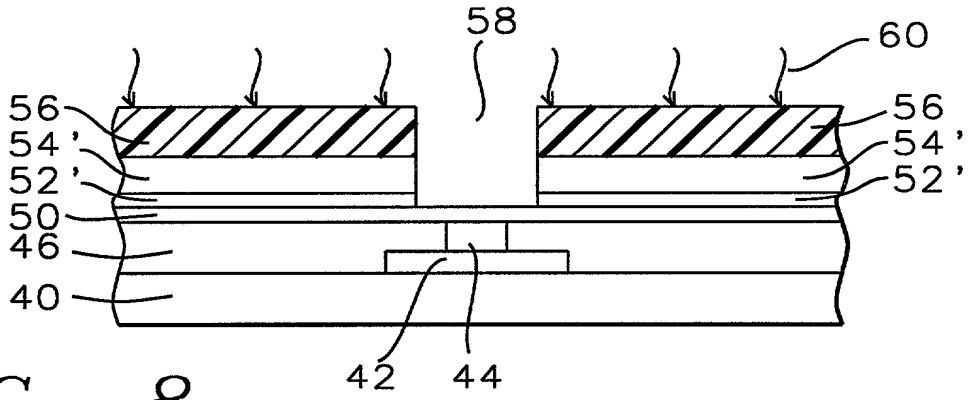


FIG. 8

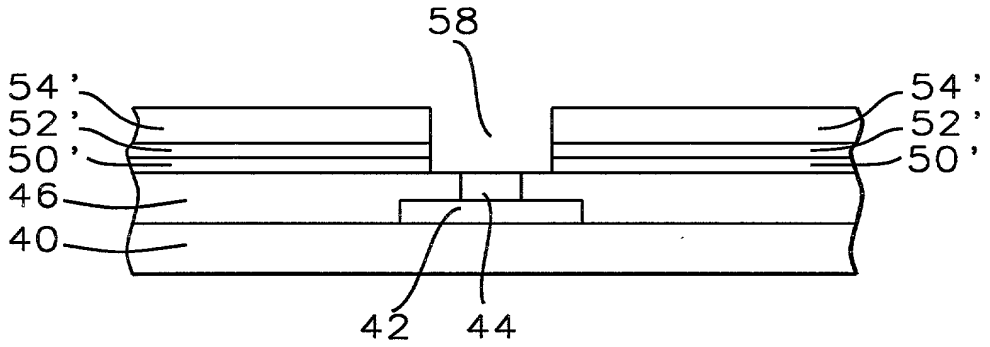


FIG. 9

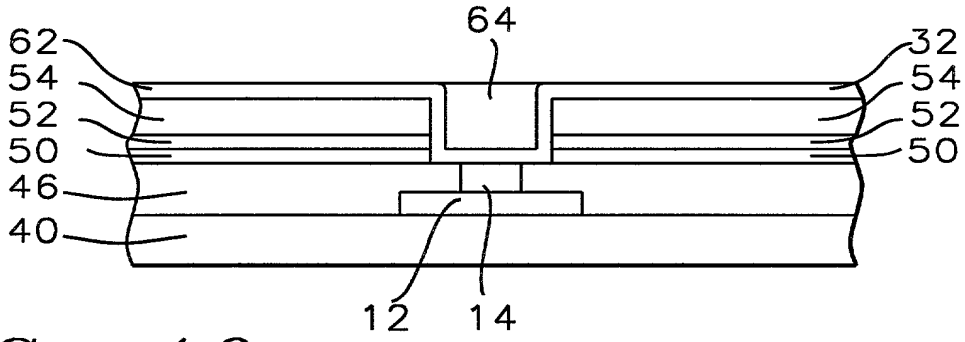


FIG. 10

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

DOCKET NO. **TS98-684/685/689**

As a below named Inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled Damascene Method Employing Composite Etch Stop Layer

the specification of which (check one)

X is attached hereto.

was filed on _____

Application Serial No. _____

and was amended on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above Identified specification including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)

		Priority Claimed:
(Number)	(Country)	(Day/Month/Year Filed)
(Number)	(Country)	(Day/Month/Year Filed)

I hereby claim the benefit under Title 35, United States Code §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (list name & registration no.)

GEORGE 0. SAILE. (Reg. No. 19,572), STEPHEN B. ACKERMAN (Reg. No. 37,761)

Send Correspondence to: 20 MCINTOSH DRIVE, POUGHKEEPSIE; NEW YORK 12603

Direct telephone Calls to: (name & telephone number) GEORGE 0. SAILE NEW YORK 914 452 5863

SYUN-MING JANG
Full name of **sole or first** inventor

Date

Inventor's signature

9. 28. '99

4F, 83 N. Kuan-Hua St., Hsin-Chu, Taiwan, ROC
Residence

Republic of China, Taiwan
Citizenship

No. 9, Creation Rd. I, Science-Based Industrial Park, Hsin-Chu, Taiwan, ROC
Post Office Address

DOCKET NO. TS98-684/685/68 S

CHUNG-SHI LIU
Full name of **second** inventor

Chung Shi Liu
Inventor's signature

Date 9.8.'99

8F-5. No. 101, Chi-Yu Rd, Hsin-Chu Taiwan
Residence

Republic of China, Taiwan
Citizenship

No. 9, Creation Rd. I, Science-Based Industrial Park, Hsin-Chu, Taiwan, R.O.C.
Post Office Address

CHEN-HUA YU
Full name of **third** inventor

Chen-hua yu
Inventor's signature

Date 9.8.'99

3F. 38 Waterfront Rd II. Hsin-Chu, Taiwan
Residence

Republic of China, Taiwan
Citizenship

9 Creation Rd. I, SBIP. Hsin-Chu. Taiwan
Post Office Address

Full name of **fourth** inventor

Date

Inventor's signature

Residence

Citizenship

Post Office Address

Full name of **fifth** inventor

Date

Inventor's signature

Residence

Citizenship

Post Office Address

Full name of **sixth** inventor

Date

Inventor's signature

Residence

Citizenship

Post Office Address